IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Currently Amended): A semiconductor memory comprising a memory cell matrix including a plurality of cell columns arranged along a row-direction, each of cell columns is implemented by a plurality of memory cell transistors serially arranged along a column-direction, the memory cell matrix comprising:

a plurality of device isolation films running along the column-direction, arranged alternatively between the cell columns;

a plurality of first conductive layers having top surfaces lower than [[the]] a level of top surfaces of the device isolation films, arranged along the row and column-directions, a group of the first conductive layers arranged along the column-direction is assigned to a corresponding cell column, adjacent groups of the first conductive layers assigned to adjacent cell columns are isolated from each other by the device isolation film disposed between the adjacent groups;

a plurality of inter-electrode dielectrics arranged selectively and respectively on [[the]] corresponding first conductive layers, the inter-electrode dielectric has a dielectric constant larger than that of silicon oxide; and

a plurality of second conductive layers running along the row-direction, each of the second conductive layers arranged on the inter-electrode dielectric and the device isolation films so that the second conductive layer can be shared by the memory cell transistors arranged along the row-direction belonging to different cell columns.

Claim 2 (Currently Amended): The semiconductor memory of claim 1, wherein each of the inter-electrode dielectrics is embedded at least a portion of a space defined by [[the]] a

top surface corresponding to a level of the top surfaces of the device isolation films and [[the]] a bottom surface corresponding to a level of the top surfaces of the first conductive layers.

Claim 3 (Currently Amended): The semiconductor memory of claim 2, wherein a thickness of the inter-electrode dielectrics is thinner than [[the]] a difference between the level of the top surfaces of the device isolation films and the level of the top surfaces of the first conductive layers, and each of [[the]] a bottom surfaces of the inter-electrode dielectrics contacts with side surfaces of the device isolation films and [[the]] a top surface of the corresponding first conductive layer.

Claim 4 (Currently Amended): The semiconductor memory of claim 3, further comprising auxiliary conductive layers filled respectively in isolated spaces, each of which are defined by [[the]] a bottom surface of [[the]] a corresponding second conductive layer and [[the]] a top surface of the corresponding inter-electrode dielectric.

Claim 5 (Original): The semiconductor memory of claim 3, wherein the thickness of each of the inter-electrode dielectrics at both edges near the device isolation film is thicker than that at central portion.

Claim 6 (Currently Amended): The semiconductor memory of claim 3, wherein each of the top surfaces of the first conductive layers manifests a curved surface such that both edges of the curved surface are higher than [[the]] a level of [[the]] a central portion of the curved surface.

Claim 7 (Currently Amended): The semiconductor memory of claim 2, wherein the space, in which the inter-electrode dielectrics is embedded, manifests a topology of a rectangular groove, whose sidewalls encroach laterally corresponding side walls of adjacent device isolation films so as to widen [[the]] a width of the rectangular groove.

Claim 8 (Currently Amended): The semiconductor memory of claim 1, wherein each of the inter-electrode dielectrics is a single layer film selected from [[the]] a group consisting of an silicon oxide film, a silicon nitride film, an aluminum oxide film, a hafnium oxide film and a zirconium oxide film or a composite film including at least one of the single layer film.

Claim 9 (Currently Amended): A method for manufacturing a semiconductor memory comprising a memory cell matrix including a plurality of cell columns arranged along a row-direction, each of cell columns is implemented by a plurality of memory cell transistors serially arranged along a column-direction, the method comprising:

forming a periodic structure implemented by first and second ridges, both running alternately along the column-direction, each of the first ridges is made of device isolation film and each of the second ridges is made of one of protruding portions of a semiconductor substrate, a cell site gate insulator on the protruding portion of the semiconductor substrate and a first conductive layer on the cell site gate insulator, [[the]] a top surface of the second ridges is lower than [[the]] a top surface of the first ridges, each of the second ridges is assigned to a corresponding cell column;

forming a plurality of inter-electrode dielectrics on [[the]] corresponding first conductive layers such that adjacent inter-electrode dielectrics are isolated by one of the first ridges, the inter-electrode dielectric has a dielectric constant larger than that of silicon oxide; and

forming a plurality of second conductive layers running along the row-direction, each of the second conductive layers arranged on the inter-electrode dielectric and the device isolation films so that the second conductive layer can be shared by the memory cell transistors arranged along the row-direction belonging to different cell columns.

Claim 10 (Currently Amended): The method of claim 9, wherein the forming inter-electrode dielectrics comprises:

blanket forming the inter-electrode dielectric so as to cover [[the]] top surfaces of the first conductive layers, [[the]] top surfaces of the device isolation films and steps defined by the top surfaces of the first and second ridges; and

planarizing [[the]] a top surface of the inter-electrode dielectric so as to expose the top surfaces of the device isolation films.

Claim 11 (Currently Amended): The method of claim 9, wherein the forming inter-electrode dielectrics comprises:

blanket forming the inter-electrode dielectric so as to cover [[the]] top surfaces of the first conductive layers, [[the]] top surfaces of the device isolation films and steps defined by the top surfaces of the first and second ridges;

blanket forming an auxiliary conductive layer on the inter-electrode dielectric; and

planarizing [[the]] a top surface of a stacked layer of the auxiliary conductive layer and the inter-electrode dielectric so as to expose [[the]] top surfaces of the device isolation films so that the auxiliary conductive layer can be selectively embedded in grooves defined by the steps.

Claim 12 (Currently Amended): The method of claim 11, after forming the periodic structure, further comprising:

etching sidewalls of device isolation films exposed at spaces implemented by the steps so as to widen [[the]] a width of the spaces,

before blanket forming the inter-electrode dielectric.

Claim 13 (Currently Amended): The method of claim 9, wherein the forming inter-electrode dielectrics comprises:

removing natural oxide films formed on surfaces of the first conductive layers by gas etching in a CVD furnace; and

forming selectively the inter-electrode dielectrics on [[the]] a top surface of the first conductive layers in the CVD furnace, keeping [[the]] a natural oxide removed surface of the first conductive layers airtight.

Claim 14 (Original): The method of claim 13, wherein the forming selectively the inter-electrode dielectrics is executed at substrate temperatures between 500°C to 700°C.

Claim 15 (Original): The method of claim 13, wherein the forming selectively the inter-electrode dielectrics is executed by CVD process using silicon halide as a source gas.

Claim 16 (Original): The method of claim 15, wherein the silicon halide is a chloride compound.

Claim 17 (Currently Amended): The method of claim 16, wherein the chloride compound is a compound selected from [[the]] a group consisting of tetrachlorosilane and trichlorosilane.

Claim 18 (Currently Amended): The method of claim 9, wherein the forming the periodic structure comprises:

forming the cell site gate insulator on the semiconductor substrate;

forming the first conductive layer on the cell site gate insulator;

forming an end point monitoring film on the first conductive layer, the end point monitoring film having different etching behavior from the device isolation film;

forming a masking film on the end point monitoring film, the masking film having the same etching behavior as the device isolation film;

delineating the masking film so as to form an etching mask;

selectively etching the end point monitoring film, the first conductive layer, the cell site gate insulator and an upper portion of the semiconductor substrate so as to form a plurality of device isolation grooves running along the column-direction, defining a plurality of the second ridges arranged alternatively between [[the]] device isolation grooves;

blanket forming the device isolation film so as to fill in the device isolation grooves;

planarizing [[the]] a top surface of the device isolation film so as to expose periodically a plurality of [[the]] top surfaces of the end point monitoring films; and

etching selectively the end point monitoring films, employing [[the]] a difference of [[the]] etching behaviors.

Claim 19 (Currently Amended): The method of claim 18, after etching selectively the end point monitoring films, further comprising:

planarizing the top surface of the device isolation film so as to expose periodically a plurality of [[the]] top surfaces of the first conductive layer; and

removing selectively [[the]] exposed top surfaces of the first conductive layers so that each of the top surfaces of the first conductive layers manifests a curved surface such that both edges of the curved surface are higher than [[the]] a level of [[the]] a central portion of the curved surface.

Claim 20 (Original): The method of claim 9, wherein each of the inter-electrode dielectrics is a single layer film selected from the group consisting of an silicon oxide film, a silicon nitride film, an aluminum oxide film, a hafnium oxide film and a zirconium oxide film or a composite film including at least one of the single layer film.